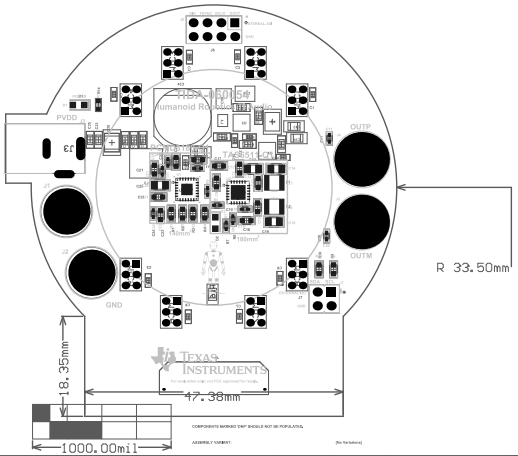
#1 ■ Install stand-to-silkscreened last after final wash. Test shall be 5 pt here. Test shall be per the Label Table in the PDF schematic.

#2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

#3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

#4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [illegible]om
PLOT NAME = L[illegible]Assembly Drawing

BOARD #: Robotics Design REV: A SVN REV: Not in version control
IID #: TIDA-060054
GENERATED : 10/26/2026 3:43:23 PM
TEXAS INSTRUMENTS

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ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

221 ■ Install stand-to-silkscreened text after final mask. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

222 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

223 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

224 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

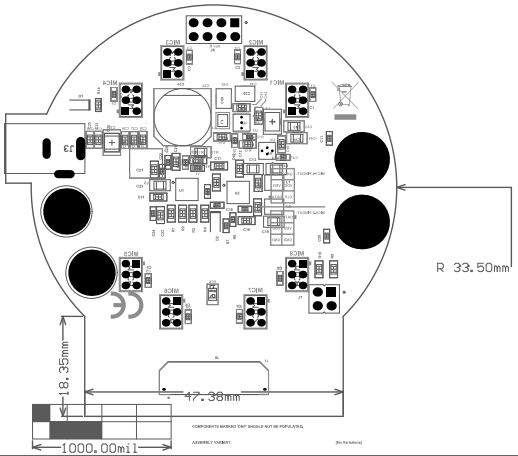
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

JUSTIFICATION FOR TOP CLICKING "PRE-DESIGNATE ENTERPRISES"

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: Robotics_Design REV: A SVN REV: Not in version control
LAYER NAME = [redacted]Bottom	TID #: TIDA-060054
PLOT NAME = L2-GND1 Assembly Drawing	GENERATED : 10/26/2026 3:43:24 PM TEXAS INSTRUMENTS

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ENGINEER:	LAYOUT BY:
Garret Godfrey	Tessolve
SCALE: 0.72	ALTIUM DESIGNER VERSION: 23.1.1.15

221 ■ Board sized to silkscreened box after final mask. Test shall be 5 pt box. Test shall be per the Label Table in the PDF schematic.
222 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
223 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
224 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

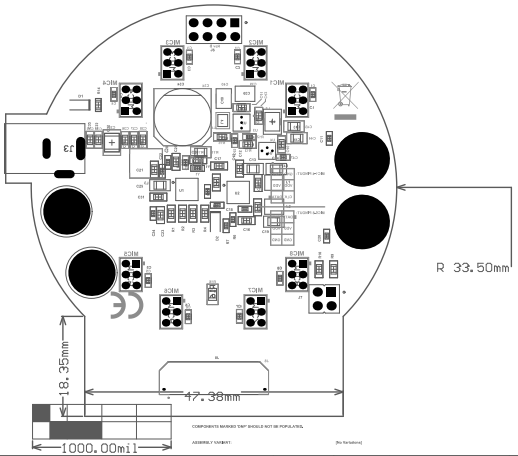
STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.
2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.
3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.
4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY+RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM- TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = L3_Signal Assembly Drawing

BOARD #: Robotics Design REV: A SVN REV: Not in version control
SID #: TIDA-060054
GENERATED : 10/26/2026 3:43:25 PM
TEXAS INSTRUMENTS

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ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

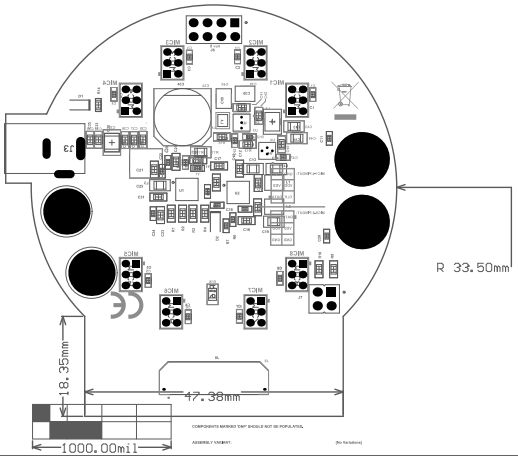
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED . PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES . MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM- TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = L6_GND2Assembly Drawing

BOARD #: Robotics_Design REV: A SVN REV: Not in version control
TID #: TIDA-060054
GENERATED : 10/26/2026 9:43:26 PM

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221 ■ Board sized to silkscreened size after final mask. Test shall be 5 pt here. Test shall be per the Label Table in the PDF schematic.

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223 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

224 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

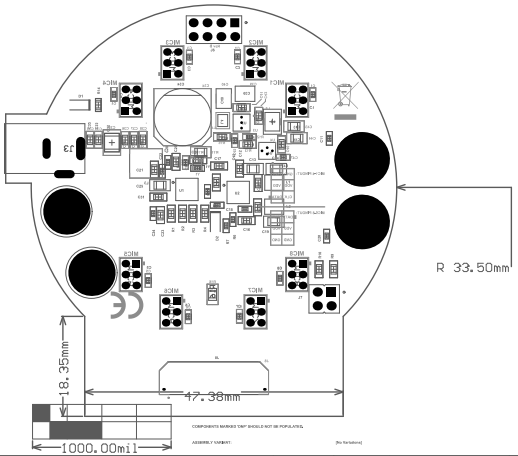
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

SOLUTION DB TOP CLOCKS *RHZ 32KHZAM-ET/EP/PWCD

[variation set off] - TRANSKY SUBSIDIER

DESIGN INFORMATION			
MIN. TRACK WIDTH:	5 MIL		
MIN. CLEARANCE:	6 MIL		
MIN. VIA PAD SIZE:	19.685 MIL		
MINIMUM ANNULAR RING	0.05mm (2MIL)	EXTERNAL	
PER	IPC-D-275 CLASS 2 LEVEL C		
REGISTRATION TOLERANCES:	METAL +/- 5 MIL, HOLES	+/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):		+/- 3 MIL	

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM- TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE

LAYER NAME = [redacted]Bottom

PLOT NAME = L5_PWR Assembly Drawing

BOARD #: Robotics Design REV: A SVN REV: Not in version control

IID #: TIDA-060054

GENERATED : 10/26/2026 9:43:28 PM

TEXAS INSTRUMENTS

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

ENGINEER: Garret Godfrey

LAYOUT BY: Tessolve

SCALE: 0.72

ALTIUM DESIGNER VERSION: 23.1.1.15

221 Board sized to allow normal box after final mask. Test shall be 5 pt box. Test shall be per the Label Table in the PDF schematic.

222 These assemblies are ESD sensitive, ESD precautions shall be observed.

223 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

224 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

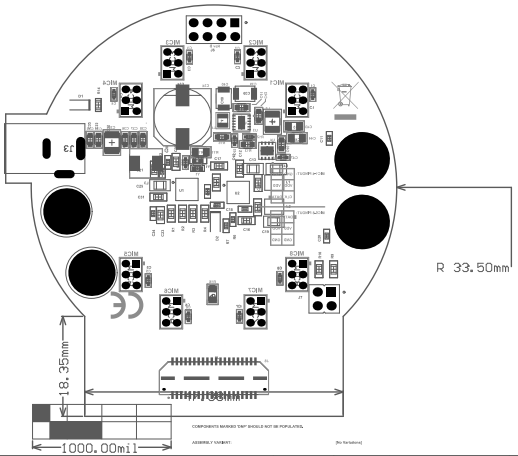
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED . PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES . MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

SOLDERMASK SHALL BE TENTED OVER EXPOSED VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL

MIN. CLEARANCE: 6 MIL

MIN. VIA PAD SIZE: 19.685 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[X] FR-4 [ ] FR-4 High Tg [ ] OTHER

THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [X] GREEN [ ] OTHER

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG

[ ] IMM- TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics_Design.PcbDoc

ENGINEER: Garret Godfrey

LAYOUT BY: Tessolve

SCALE: 0.72

ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE

LAYER NAME = [redacted]Bottom

PLOT NAME = L6_BottomAssembly Drawing

BOARD #: Robotics Design REV: A SVN REV: Not in version control

DID #: TIDA-060054

GENERATED : 10/26/2026 - 3:43:29 PM

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